the input switches through six first internal links (for example the links FL1-FL6 connected to the middle switch MS1 from each of the input switch IS1-IS6), and connected to each of the output switches through six second internal links (for example the links SL1-SL6 connected from the middle switch MS1 to each of the output switch OS1-OS6). In one embodiment, the network also includes a controller coupled with the input stage 110, output stage 120 and middle stage subnetworks 130 to form connections between an inlet links IL1-IL12 and an arbitrary number of outlet links OL1-OL12.

Each of middle switches MS1-MS5 is a $V(5,2,3)$ three-stage subnetwork. For example, the three-stage subnetwork MS1 comprises input stage of three, two by five switches MIS1-MIS3 with inlet links FL1-FL6, and an output stage of three, five by two switches MOS1-MOS3 with outlet links SL1-SL6. The middle stage of MS1 consists of five, three by three switches MMS1-MMS5. Each of the middle switches MMS1-MMS5 are connected to each of the input switches MIS1-MIS3 through three first internal links (for example the links MFL1-MFL3 connected to the middle switch MMS1 from each of the input switch MIS1-MIS3), and connected to each of the output switches MOS1-MOS3 through three second internal links (for example the links MSL1-MSL3 connected from the middle switch MMS1 to each of the output switch MOS1-MOS3). In similar fashion the number of stages can increase to 7, 9, etc.

As with the three-stage network, the network of FIG. 5A has the property of being operable in strictly nonblocking manner as described herein with no more than $3*n-1$ middle stage three-stage networks. In the network of FIG. 5A the middle stage requires no more than $3*n-1$ three-stage subnetworks. Thus in FIG. 5A where n equals 2, middle stage 130 has five middle stage three-stage subnetworks MS1-MS5. Furthermore, according to the present invention, each of the middle stage subnetworks MS1-MS5 require no more than $2*k_1+k_2-1$ middle switches MMS1-MMS5, where k_1 is the number of inlet links for each middle input switch MIS1-MIS3 and k_2 is the number of outlet links for each middle output switch MOS1-MOS3.

In general, according to certain embodiments, one or more of the switches, in any of the first, middle and last stages can be recursively replaced by a three-stage subnetwork with no more than $2*n_1+n_2-1$ middle stage switches where n_1 is the

number of inlet links to the first stage switch in the subnetwork and n_2 is the number of outlet links to the last stage switch of the subnetwork for strictly nonblocking operation, for multicast connections of arbitrary fan-out. Note that because the term "subnetwork" has the same meaning as "network", the just described replacement can be repeated recursively, as often as desired, depending on the embodiment.

It should be understood that the methods, discussed so far, are applicable to k-stage networks for k>3 by recursively using the design criteria developed on any of the switches in the network. The presentation of the methods in terms of three-stage networks is only for notational convenience. That is, these methods can be generalized by recursively replacing each of a subset of switches (at least 1) in the network with a smaller three-stage network, which has the same number of total inlet links and total outlet links as the switch being replaced. For instance, in a three-stage network, one or more switches in either the input, middle or output stages can be replaced with a three-stage network to expand the network. If, for example, a five-stage network is desired, then all middle switches (or all input switches or all output switches) are replaced with a three-stage network

In accordance with the invention, in any of the recursive three-stage networks each connection can fan out in the first stage switch into at most two middle stage subnetworks, and in the middle switches and last stage switches it can fan out any arbitrary number of times as required by the connection request. For example as shown in the network of FIG. 5A, connection I_1 fans out in the first stage switch IS1 once into middle stage subnetwork MS1. In middle stage subnetwork MS1 it fans out four times into output switches OS1, OS2, OS3 and OS5. In output switches OS1 and OS3 it fans out twice. Specifically from output switch OS1 into outlet links OL1, OL2, and from output switch OS3 into outlet links OL5, OL6. In output switches OS2 and OS5 it fans out once into outlet links OS4 and OS9 respectively. However in the three-stage network MS1, it can fan out at most twice in the first stage, for example connection I_1 fans out twice in the input switch MIS 1 into middle switches MMS2 and MMS3 of the three-stage subnetwork MS1. Similarly a connection can fan out arbitrary number of times in the middle and last stages of any three-stage subnetwork. For example connection I_1 fans out twice in middle switch MMS2 into output switches MOS1 and MOS2 of three-stage

subnetwork MS1. In the output switch MOS1 of three-stage subnetwork MS1 it fans out twice into output switches OS1 and OS2. And in the output switch MOS2 of three-stage subnetwork MS1 it fans out once into output switch OS3. Also the connection I_1 fans out in middle switch MMS3 once into output switch MOS2 of the three-stage subnetwork MS1 and from there once into output switch OS5.

The connection I_3 fans out once into three-stage subnetwork MS3 where it is fanned out three times into output switches OS2, OS4, and OS6. In output switches OS2, OS4, and OS6 it fans out once into outlet links OL3, OL8, and OL12 respectively. The connection I_3 fans out once in the input switch MIS7 of three-stage subnetwork MS3 into middle switch MMS12 of three-stage subnetwork MS3 where it fans out three times into output switches MOS7, MOS8, and MOS9 of the three-stage subnetwork MS3. In each of the three output switches MOS7, MOS8 and MOS9 of the three-stage subnetwork MS3 it fans out once output switches OS2, OS4, and OS6 respectively.

FIG. 5B shows a high-level flowchart of a rearrangeable scheduling method, in one embodiment executed by the controller of FIG. 5A. The method of FIG. 5B is used only for networks that have three stages each of which may be in turn composed of three-stage subnetworks, in a recursive manner as described above in reference to FIG. 5A. According to this embodiment, a multicast connection request is received in act 250 (FIG. 5B). Then a connection to satisfy the request is set up in act 260 by fanning out into at most two middle stage subnetworks from its input switch. Then the control goes to act 270. Act 270 recursively goes through each subnetwork contained in the network. For each subnetwork found in act 270 the control goes to act 280 and each subnetwork is treated as a network and the scheduling is performed similarly. Once all the recursive subnetworks are scheduled the control transfers from act 270 to act 250 so that each multicast connection will be scheduled in the same manner in a loop.

A direct extension of the foregoing discussion is that when the number of middle switches is increased, the above-described methods can be changed to improve speed. For example when $m = 4 * n - 1$, each multicast connection can be fanned out into at most three middle switches and the $V(m,n,r)$ network can be operated in strictly nonblocking manner. Similarly, when $m = 3 * n_1 + n_2 - 1$, the $V(m,n_1,r_1,n_2,r_2)$ network is operated in